REMARKS

In the Detailed Action of the current Final Office Action, **claims** 1-5, 18, and 20-22 are newly **rejected using,** inter alia, **newly cited prior art** (e.g., Jones et al. (U.S. 5,548,181)). In this circumstance, Applicants respectfully request that the finality of the current Office Action be withdrawn, as none of those claims were amended as part of the previous submission by Applicants nor was any IDS recently provided (MPEP 706.07(a)).

Claim Rejection Under 35 U.S.C. 102

Claims 1, 3, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Jones et al. (U.S. 5,548,181). Applicants respectfully traverse this rejection.

Claim 1 recites in part:

> ... **a shadow mask including a plurality of openings defined therethrough according to a predetermined pattern** ...; and
>
> **an insulative layer including a first portion formed on the upper surface of the shadow mask, a plurality of second portions, and a third portion formed on the lower surface of the shadow mask,** the second portions disposed in the respective openings and connecting the first portion with the third portion. (Emphasis added.)

Jones et al. discloses that a spacer incorporates an insulator, which is made of a silica material and coated with a low electron emission coating

such as magnesium oxide (MgO), and a buried conductor formed of a suitable material, such molybdenum or aluminum, and connected to ground. FIG. 74 of Jones et al. further shows that the conductor is disposed under the insulator and that the low electron emission coating is formed on an upper surface of the insulator, inner edges of the insulator and the conductor, and a lower surface of the conductor. However, Jones et al. fails to disclose or suggest a shadow mask and an insulative layer with the insulative layer being formed on each of an upper surface and a lower surface of the shadow mask, as essentially required by claim 1.

Indeed, Jones et al. discloses a conductor and an insulator coating with a low electron emission coating that covers an upper surface of the insulator and a lower surface of the conductor. **Even if** the buried conductor and the low electron emission coating are, respectively, considered to be a shadow mask and an insulative layer, **as is contended by the Examiner in the Office Action, no insulative layer is formed on upper surface** of the conductor because of the arrangement of the insulator between the conductor and the low electron emission coating. Thus, Jones et al. fails to disclose or suggest a shadow mask; and an insulative layer formed on upper and lower surfaces of the shadow mask and, therefore, neither anticipates nor renders obvious the subject matter of claim 1.

Therefore, claim 1 is not taught, or suggested by Jones et al. or any of the other cited references, taken alone or in combination.

Furthermore, the shadow mask of the presently claimed device produces new and unexpected results. A shadow mask used in the device of claim 1 can be made by a known technology in the flat panel display field

with a high precision, and the claimed barrier array is convenient and inexpensive to make. Additionally, no insulator is disposed between the shadow mask and the insulative layer of claim 1, thereby decreasing the cost of the fabrication of the presently claimed device. Therefore, claim 1 is patentable over Jones et al. under U.S.C. 102 and 103.

Accordingly, claim 1 is in condition for allowance, the allowance of which is hereby respectfully requested.

Claim 3 is directly dependent from now-allowable claim 1, and, as such, Applicants submit that claim 3 should also be allowable.

Claim 18 recites in part:

> ...**a metal plate including a plurality of openings therethrough according to a pixel pattern of a flat panel display**, the metal plate having an upper surface and a lower surface opposite to the upper surface; and
>
> **an insulative layer including a first portion formed on the upper surface** of the metal plate **and a plurality of second portions, the second portions extending** from the first portion **into the respective openings and formed on inner edges of the metal plate that bound the respective openings.** (Emphasis added.)

For similar reasons asserted with respect to claim 1, the low electron emission coating disclosed by Jones et al. is not formed on the upper surface of the conductor because of the insulator is disposed between the conductor and the lower electron emission coating. Thus, Jones et al. fails to disclose

or suggest a metal plate and an insulative layer that is formed on upper surface and inner edges of the metal plate, as required by claim 18.

Therefore, claim 18 is not taught or suggested by Jones et al. or any of the other cited references, taken alone or in combination.

Furthermore, the metal plate and the insulative layer of the present invention, as provided in claim 18, produce new and unexpected results, as set forth above with respect to claim 1. Therefore, claim 18 is patentable over Jones et al. under U.S.C. 102 and 103.

Accordingly, claim 18 is in condition for allowance, the allowance of which is hereby respectfully requested.

Claim 20 is directly dependent from claim 18, and, as such, Applicants submit that claim 20 should also be allowable.

Claim Rejection Under 35 U.S.C. 103

(i) Claims 4, 5 and 22 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Jones et al. (U.S. 5,548,181).

Claims 4 and 5 are each directly dependent from claim 1. As detailed above, claim 1 is submitted to be patentable over Jones et al. under 102 and 103. Therefore, claims 4 and 5 should also be allowable, since each of them includes the patentably distinguishing features of claim 1.

Claim 22 is directly dependent from claim 18. As detailed above,

claim 18 is submitted to be patentable over Jones et al. under 102 and 103. Therefore, claim 22 should also be allowable, since it includes the patentably distinguishing features of claim 18.

(ii) Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. 5,548,181) in view of Lee et al. (U.S. 6,508,685B1; of record).

Claim 2 is directly dependent from claim 1. As detailed above, claim 1 is submitted to be patentable over Jones et al. under 102 and 103. Therefore, claim 2 should also be allowable, since it includes the patentably distinguishing features of claim 1.

In view of the foregoing, the present application as defined in the pending claims is considered to be in a condition for allowance, and an action to such effect is earnestly solicited.

Applicant respectfully notes that any new grounds of rejection in a next Office Action could not be considered as having been necessitated by amendment or by an Information Disclosure Statement. Accordingly, if the next Office Action includes such a rejection, it would not be proper for that Action to be made Final, as per the guidelines set forth in MPEP 706.07(a).

Respectfully submitted,

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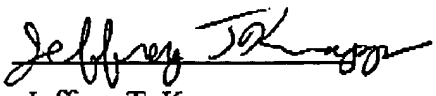
By 

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